Leading Scholar and Scientist in the field of electronics engineering, founder of national VLSI Design and Education Center at the University of Tokyo, author of several course books in engineering in Japan visits Istanbul and gives talk at Bahcesehir University!

**Date:** October 20, 2011, **Thursday** 15:00 – 17:00  
**Place:** Fazil Say Consortium, Bahcesehir University, Besiktas, Istanbul

**Summary of the Talk**

The unstable/unpredictable LSI operation caused by the PVT (Process Voltage Temperature) variations, along with the aging effect such as NBTI/PBTI, is one of the serious issues in current and future scaled LSIs. In these situations, where operation environments in the field are hard to predict at the stages of circuit design and test, the errors are revealed mainly as the delay faults. The conventional approach of the margin-based design and test in the synchronous architecture has to pay a large amount of penalty in operation speed in order to guarantee the safe operation. This presentation shows recent results of self-synchronous circuits studied in our research group, focusing on Self-Synchronous FPGA (SS-FPGA), after summarizing several solutions in the synchronous approaches and their weak points. The SS-FPGA is designed to be robust for PVT variations and the aging effect without paying so much speed penalty. **Keywords-Self-synchronous, completion detection, error detection, PVT variation, aging, delay-fault, pipeline, FPGA**

**Biography**

Kunihiro Asada was born in Fukui, Japan. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from University of Tokyo, Japan, in 1975, 1977, and 1980, respectively. In 1980, he joined the Faculty of Engineering, University of Tokyo, and became a Lecturer, an Associate Professor, and a Professor in 1981, 1985, and 1995. From 1985 to 1986, he stayed at Edinburgh University as a Visiting Scholar supported by the British Council. In 1996, he established the VLSI Design and Education Center (VDEC) with his colleagues at the University of Tokyo, which is a center to promote education and research of VLSI design in all the universities and colleges in Japan. He is currently Director of VDEC. His research interests include design and evaluation of integrated systems and component devices. He has published more than 400 technical papers in journals and conference proceedings. Dr. Asada served as the first Editor of the English version of IEICE (Institute of Electronics, Information and Communication Engineers of Japan) Transactions on Electronics, as the Chair of IEEE/SSCS Japan Chapter and the Chair of IEEE Japan Chapter Operation Committee. He has received best paper awards from the Institute of Electrical Engineers of Japan, IEICE, and ICMTS1998/IEEE. He is a member of IEICE and IEEJ.